ENSONIQ AudioPCI™ ES1370

Preliminary Specification

1.INTRODUCTION

AudioPCI™ ES1370 is a new ENSONIQ device that provides the next generation of audio performance to the PC market. AudioPCI™ ES1370 is a 5.0 Volt PCI bus compatible device that enables the ENSONIQ SoundScape PCI solution. AudioPCI™ ES1370 along with a 16 bit CODEC offer the next generation of audio performance in a PC while maintaining full legacy compatibility without old ISA bus solutions. Some of the capabilities of AudioPCI™ are:

·SoundScape WaveTable synthesizer .

·Multiple sample rate support

·PCI Bus Master for fast DMA

·Sounds are stored in Main memory.

·Access to Ensoniq's World Famous Sound Library of over 4000 Sounds

·3 Stereo inputs and 3 mono inputs can be mixed into the output stream.

·Direct I/O space access of the control registers.

·100 Pin PQFP or TQFP

·External MPEG/DVD (I2S) input

·No ISA bus pins required

·4 speaker output capability for Surround Sound environment

·On board selectable 30dB/0dB gain mic preamp

·Software Controlled Power Management

1.DESIGN CONCEPT

The AudioPCI™ ES1370 is a PCI bus master and slave device that is best understood by looking at the device as four interactive subsystems: the PCI interface, DMA control, Legacy functions, and the CODEC.

1.1.PCI Interface

The PCI subsystem is a bus master interface that performs the memory accesses to keep the Audio cache buffers full and empties the A/D Converter and MPEG buffers to main memory as required.

The fundamental concept of AudioPCI™ is that the PCI interface controller has a sufficiently large internal (on-chip) memory cache to meet the memory bandwidth requirements. There is a Sound Cache block of 64 bytes for each of the audio channels. It is the responsibility of the DMA control and the software to keep the buffers full.

All system control registers are accessed via I/O on the PCI bus. AudioPCI™ uses 16 Long Words in the I/O space for control registers. All registers are read as Long Words. All registers are written in byte or word format.

1.2.LEGACY

The Legacy subsystem is the circuitry required to perform SoundBlaster, OPL-FM and MPU-401 emulation. Functionally AudioPCI™ traps on access of the SoundBlaster registers and then issues the appropriate IRQ or SERR command on the PCI bus. AudioPCI™ handles the Legacy DMA function in a similar fashion. The exact functionality of the block cannot be fully disclosed at this time due to pending patent protection for the application of this technique.

1.3.CODEC

The Codec is the Asahi Kasei 4531. The functionality of the A/D and D/A sections are similar to those found in other standard CODECs. The A/D portion of the Codec is handled as an independent asynchronous event with a DMA buffer control structure. Each time the A/D FIFO is filled, a Bus Master request occurs and the FIFO is transferred to main memory.

2.BLOCK DIAGRAM

THE SYSTEM Components

2.1.Bus Master Cache Control (CCB)

This block controls the transfer of data between the PCI memory and the internal memory. The Serial block signals when a cache fill is required in the three memory buffers. The CCB calculates the PCI address from the frame data and issues a command to the PCI interface. When the PCI interface signals that the data is available the CCB channels the data to the proper place in memory. This block is functionally equivalent to a 3 channel DMA controller.

2.2.Serial Input Block

This block performs serial to parallel conversion and parallel to serial conversion for the record and playback channels respectfully. The record channel source can be either the MPEG or CODEC ADC serial input signals. This block also signals the CCB block when a cache fill is required.

2.3.Host Interface

This block arbitrates a PCI access to the high speed internal memory. When the data transfer is complete, it responds with an acknowledge to the PCI interface block.

2.4.CODEC Interface

This block Reads/writes configuration data from the host bus to the CODEC using the serial protocol of the CODEC. This block also switches and modifies the serial clocks required by the serial block and the CODEC.

2.5.IRQ & Chip Select Block

The functions for this block are:

1.Decode the internal address bus to generate chip selects to each block.

2.Contains internal registers whose outputs are control bits used by internal blocks for control/selection.

3.Summarizes all system IRQ's (UART, CODEC, etc.) to generate a single AudioPCI™ IRQ to the host. This also includes the playback and record DMA channels. Any IRQ masking is performed within the individual blocks except for the CCB block interrupt.

4.For Platform designs, the PCI SERR# pin of AudioPCI™ is connected to the PCI Chip set NMI output, and the EXT_IRQ is connected to the CPU NMI.

0.1.Legacy Block

This block generates IRQ or SERR# at a specified ADLib access, SoundBlaster access, DMA controller access, IRQ (PIC) controllers access, Microsoft WSS access, or Soundscape access.

0.2.High Speed Memory Bus

This pathway is used exclusively to transfer data between the internal memory and the various sub-systems. The access priority for this bus is (highest to lowest):

Cache Control block
Host Interface
UART interface
Serial Output and A/D Control

0.3.Internal Memory

The internal memory in AudioPCI™ is organized as 4 blocks of 64 bytes each. Each block is divided into 4 pages of 16 bytes each (4 longwords). Memory can be accessed as longwords only. In order to access a specific page of memory the memory page register must first be setup for the specific page to be accessed. The first three blocks of memory contain the 3 circular buffers for the 2 playback channels and the record channel. The last block contains the frame information for the playback and record channels and also includes the UART FIFO. The memory block and page organization is shown below :

Block PageHigher AddressLower

0 - DAC 1	0000	DAC1 sample bytes 15 - 0 Lower half buffer
	0001	DAC1 sample bytes 31 - 16
	0010	DAC1 sample bytes 47 - 32 Upper half buffer
	0011	DAC1 sample bytes 63 - 48
1 - DAC2	0100	DAC2 sample bytes 15 - 0 Lower half buffer
	0101	DAC2 sample bytes 31 - 16
	0110	DAC2 sample bytes 47 - 32 Upper half buffer
	0111	DAC2 sample bytes 63 - 48
2 - ADC	1000	ADC sample bytes 15 - 0 Lower half buffer
	1001	ADC sample bytes 31 - 16
	1010	ADC sample bytes 47 - 32 Upper half buffer
	1011	ADC sample bytes 63 - 48
3 - Frame/UART	1100	DAC1, DAC2 frame information (see register descriptions)
	1101	ADC frame information (plus 2 open longwords)
	1110	UART fifo (only bits 8 - 0 of each longword are used)
	1111	UART fifo

1.PCI Data Transfers

The internal control registers of the AudioPCI Chip and the CODEC are accessed via 16 Long Words in PCI direct I/O space. These registers are read as 32 bit quantities and written as byte, word or longword entities. PCI bus mastering is used to transfer audio data between system memory and AudioPCI internal memory. The internal Cache Control Block and the PCI Interface control these transfers. Only burst read/write transfers are required. All data transfers are 8 Long Word burst transfers.

1.1.Audio Read Transfers

The CCB requests a read data transfer from the PCI interface block (PCIB). The PCIB arbitrates for the PCI bus and initiates an 8 long word read starting at the system address specified by the CCB in the read request. When the data is acquired, the PCIB signals the CCB to begin moving the data to internal memory. The CCB performs any byte alignment required and writes the data to the appropriate buffer in the internal memory. The CCB will complete the current transfer request and then proceed to the next highest priority request.

1.2.Audio Write Transfers

The CCB will first write up to 8 long words into the intermediate PCI buffer. The CCB will then request a write transfer from the PCIB to main memory and specify the starting address of the transfer. The PCIB arbitrates for the PCI bus and transfers 8 Long Words into system memory. Eight Long words will always be transferred during this operation.

2.PCI CONFIGURATION SPACE

The following information is the PCI configuration space for the AudioPCI chip. All bits not specifically mentioned below are zero and read only.

Vendor IDAddress 00H
Addressable as word
Configuration Space

Bit(s)	R/W	Name	Data Value
15:0	R	VENDOR ID	1274H

Device IDAddress 02H
Addressable as word
Configuration Space

Bit(s)	R/W	Name	Data Value
15:0	R	DEVICE ID	5000H

Command Address 04H
Addressable as word

Configuration Space

Bit(s)	R/W	Name	Data Value
0,2,8	R/W	COMMAND	Variable
1,3,4, 5,6,7, 9-15	R	ZERO	Zero

Status Address 06H

Addressable as word

Configuration Space

Bit(s)	R/W	Name	Data Value
15	R	ZERO	Zero
14:12	R	ACTIVE	Variable (zero at startup)
11	R	ZERO	Zero
10:9	R	FIXED	10b
8	R	ACTIVE	Variable (zero at startup)
7:0	R	ZERO	Zero

Class Code & Revision ID Address 08H

Addressable as longword

Configuration Space

Bit(s)	R/W	Name	Data Value
31:0	R	CLASS CODE / REVISION ID	04010000H (multimedia audio device)

Cache Line SizeAddress 0CH

Addressable as Byte

Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	CACHE LINE SIZE	00H

Latency TimerAddress 0DH

Addressable as byte

Configuration Space

Bit(s)	R/W	Name	Data Value
7:3	R/W	LATENCY	Variable

2:0	R	ZERO	Zero

Header TypeAddress 0EH

Addressable as byte

Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	HEADER TYPE	00H

BISTAddress 0FH

Addressable as byte

Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	BIST	00H

Base Address Address 10H

Addressable as longword

Configuration Space

Bit(s)	R/W	Name	Data Value
31:16	R	ZERO	Zero
15:6	R/W	BASE ADDRESS	Variable
5:1	R	ZERO	Zero (address 64 byte aligned)
0	R	ONE	One

Base Address Address 14, 18, 1C, 20, 24H

Addressable as longword

Configuration Space

Bit(s)	R/W	Name	Data Value
31:0	R	Unimplemented	00000000H

Cardbus CIS Pointer Address 28H

Addressable as longword

Configuration Space

Bit(s)	R/W	Name	Data Value
31:0	R	Unimplemented	00000000H

Subsystem Vendor IDAddress 2CH

Addressable as word

Bit(s)	R/W	Name	Data Value
15:0	R	SUBSYSTEM VENDOR ID	4942H

Subsystem IDAddress 2EH
Addressable as word
Configuration Space

Bit(s)	R/W	Name	Data Value
15:0	R	SUBSYSTEM ID	4C4CH

Expansion ROM Address Address 30H
Addressable as longword
Configuration Space

Bit(s)	R/W	Name	Data Value
31:0	R	EXP ROM ADDR	00000000H

Interrupt LineAddress 3CH
Addressable as byte
Configuration Space

Bit(s)	R/W	Name	Data Value
7:4	R	ZERO	Zero
3:0	R/W	INTERRUPT	Variable

Interrupt PinAddress 3DH
Addressable as byte
Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	INTERRUPT PIN	01H

Min_GntAddress 3EH
Addressable as byte
Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	MIN_GNT	0CH

Max_LatAddress 3FH
Addressable as byte

Bit(s)	R/W	Name	Data Value
7:0	R	MAX_LAT	80H

3.REGISTER MAP

All Control registers in AudioPCI™ are addressed in the direct PCI I/O space. There are control registers for each of the major blocks of the AudioPCI™ system. The memory map is shown below:

AudioPCI™ Memory Map

Base Address	Upper Address	Module
00H	07H	Interrupt/Chip Select
08H	0BH	UART
0CH	0FH	Host Interface - Memory Page
10H	17H	CODEC Interface
18H	1FH	Legacy
20H	2FH	Serial Interface
30H	3FH	Host Interface - Memory

3.1.IRQ & Chip Select Block

The IRQ/Chip Select block contains two 32 bit registers. The first register is the control which can be read and written. The second register is the status register which is a read only register.

Interrupt/Chip Select Control Register Address 00H
Addressable as byte, word, longword
Power on reset value 00000001H Direct Mapped

Bit(s)	R/W	Name	Function
31	R/W	ADC_STOP	This bit enables the CCB block to transfer the record buffer to system memory. 0 - Record buffer transfers enabled. 1 - Record buffer transfers disabled (ADC stopped).
30	R/W	XCTL1	This is a general purpose output bit which is brought out to an external pin on the AudioPCI™ chip. This output bit is controlled

			by the SERR_DISABLE control bit (bit 0). SERR_DISABLE = 0 , XCTL1 = general purpose output bit. SERR_DISABLE = 1 , XCTL1 = external irq output (mnmi).
29	R/W	OPEN	This bit is not used but can be read or written.
28:16	R/W	PCLKDIV[12:0]	These bits are the 13 bits that set the programmable clock divide ratio. This clock is normally used as the source for the CODEC DAC (DAC2).
15	R/W	MSFMTSEL	This bit selects the MPEG serial data format. 0 - SONY (lrclk high = left channel ; data left justified) 1 - I2S (lrclk low = left channel ; data 1 bit clock delayed)
14	R/W	M_SBB	This bit selects either MPEG or Programmable clock generator as the source for the CODEC DAC. 0 - Programmable clock generator 1 - MPEG clocks
13:12	R/W	WTSRSEL[1:0]	These two bits select the sample rate from the Fixed frequency clock generator. This clock generator is the source for the CODEC FM DAC (DAC1). 00 - 5.512 Khz 01 - 11.025 Khz 10 - 22.05 Khz 11 - 44.1 Khz
11	R/W	DAC_SYNC	This bit selects whether both CODEC DAC's will run in sync off the Fixed frequency clock generator. 0 - CODEC DAC's are not synchronous 1 - CODEC DAC's are synchronous (CODEC DAC must be set to run off the clock 1 source)
10	R/W	CCB_INTRM	This bit is the interrupt mask bit for the CCB module voice interrupts. 0 - CCB voice interrupts are disabled 1 - CCB voice interrupts are enabled
9	R/W	M_CB	This bit selects either MPEG or the CODEC ADC as the source for the record channel in the serial module. 0 - CODEC ADC is record channel source 1 - MPEG is record channel source
8	R/W	XCTL0	This is a general purpose output bit which is brought out to an external pin on the AudioPCI™ chip.
7	R/W	BREQ	This bit controls access to the internal memory. It is for test purposes only. If this bit is ever set high it will prevent the CCB and Serial modules from accessing the memory. 0 - Memory bus request disabled (power on state) 1 - Memory bus request enabled (disables memory access)

6	R/W	DAC1_EN	This bit enables the DAC1 playback channel (CODEC FM DAC). To restart a channel that had stopped, this bit must be reset low and then set high. 0 - DAC1 playback channel disabled 1 - DAC1 playback channel enabled
5	R/W	DAC2_EN	This bit enables the DAC2 playback channel (CODEC DAC). To restart a channel that had stopped, this bit must be reset low and then set high. 0 - DAC2 playback channel disabled 1 - DAC2 playback channel enabled
4	R/W	ADC_EN	This bit enables the ADC playback channel (CODEC ADC). To restart a channel that had stopped, this bit must be reset low and then set high. 0 - ADC record channel disabled 1 - ADC record channel enabled
3	R/W	UART_EN	This bit enables UART module operation. 0 - UART disabled 1 - UART enabled
2	R/W	JYSTK_EN	This bit enables Joystick module operation. 0 - Joystick disabled 1 - Joystick enabled
1	R/W	CDC_EN	This bit enables CODEC interface module operation. 0 - CODEC interface disabled 1 - CODEC interface enabled
0	R/W	SERR_DISABLE	This bit enables the internal PCI module serr bus signal to be passed through to the PCI bus. 0 - PCI serr signal is passed through to PCI bus 1 - PCI serr signal is disabled

Interrupt/Chip Select Status RegisterAddress 04H

Addressable as longword only

Power on reset value 00000000000000000000??001100000bDirect Mapped

Bit(s)	R/W	Name	Function
31	R	INTR	This bit is the summary interrupt bit. 0 - No interrupt pending 1 - Interrupt from DAC1, DAC2, ADC, UART or CCB has occurred
30:11	R	ZERO	These bits always read back as zeros.

10	R	CSTAT	This bit is a summary bit for the CODEC status bits cbusy and cwrip. 0 - CODEC is not busy and no CODEC write in progress 1 - CODEC is either busy or a register write is in progress
9	R	CBUSY	This bit indicates whether the CODEC is busy or not. 0 - CODEC is not busy 1 - CODEC is busy
8	R	CWRIP	This bit indicates whether a CODEC register write is in progress 0 - CODEC write not in progress 1 - CODEC write is in progress
7	R	ZERO	This bit always reads back as a zero.
6:5	R	VC[1:0]	These bits are the voice code from the CCB module. These bits are only valid if the CCB interrupt bit (mccb) is high. 00 - DAC1 01 - DAC2 10 - ADC 11 - Undefined
4	R	MCCB	This bit is the masked CCB interrupt bit. A CCB interrupt will occur if a PCI bus abort condition occurs during a voice buffer transfer. The CCB interrupt is masked with the CCB interrupt mask bit (ccb_intrm) in the control register. 0 - No CCB interrupt 1 - CCB interrupt pending
3	R	UART	This bit is the UART interrupt bit. 0 - No UART interrupt 1 - UART interrupt pending
2	R	DAC1	This is the DAC1 playback channel interrupt bit. 0 - No DAC1 channel interrupt 1 - DAC1 channel interrupt pending
1	R	DAC2	This is the DAC2 playback channel interrupt bit. 0 - No DAC2 channel interrupt 1 - DAC2 channel interrupt pending
0	R	ADC	This is the ADC record channel interrupt bit. 0 - No ADC channel interrupt 1 - ADC channel interrupt pending

3.2.UART

The UART contains three 8 bit registers. The data register can be read or written and is used to receive or transmit MIDI information. The second register is a 8 bit control register which is write only. The third register is a 8 bit status register which is read only.

UART Data RegisterAddress 08H
Addressable as byte only
Power on reset value ??HDirect Mapped

Bit(s)	R/W	Name	Function
7:0	R/W	DATA[7:0]	The UART data register provides access to MIDI serial data input/output.

UART Status RegisterAddress 09H
Addressable as byte only
Power on reset value 00HDirect Mapped

Bit(s)	R/W	Name	Function
15	R	RXINT	This bit is the UART receiver interrupt bit. 0 - No UART receiver interrupt 1 - UART receiver interrupt pending
14:11	R	ZERO	These bits always read back as zeros to allow for soundscape detection.
10	R	TXINT	This bit is the UART transmitter interrupt bit 0 - No UART transmitter interrupt 1 - UART transmitter interrupt pending
9	R	TXRDY	This bit is the UART transmitter ready bit. 0 - UART transmitter not ready 1 - UART transmitter ready
8	R	RXRDY	This bit is the UART receiver ready bit. 0 - UART receiver not ready 1 - UART receiver ready

UART Control RegisterAddress 09H
Addressable as byte only
Power on reset value 00HDirect Mapped

Bit(s)	R/W	Name	Function
15	W	RXINTEN	This bit is the UART receiver interrupt enable bit. 0 - UART receiver interrupts disabled 1 - UART receiver interrupts enabled
14:13	W	TXINTEN[1:0]	These two bits are the control bits for the UART transmitter operation.

			00 - 01 - Txrdy interrupts enabled 10 - 11 -
12:10		UNDEFINED	These bits are undefined
9:8	W	CNTRL[1:0]	These two bits are the control bits for the UART. 00 - 01 - 10 - 11 - Software Reset

UART Reserved RegisterAddress 0AH
Addressable as byte only
Power on reset value 00HDirect Mapped

Bit(s)	R/W	Name	Function
7:1		UNDEFINED	These bits are undefined.
0	R/W	TEST_MODE	This bit enables the UART test mode. When the test mode bit is set the UART clock is switched to the PCI bus clock. The faster clock reduces the size of the test vectors and also shortens the run time of the test vectors. The power up state is normal mode enabled. 0 - Normal mode enabled. 1 - UART test mode enabled.

3.3.Host Interface - Memory Page

The memory page register is a four bit register used to access one of 16 memory pages within the AudioPCI[TM] chip. This register can be read or written but any unused bits are undefined on read back.

Memory Page RegisterAddress 0CH
Addressable as byte, word, longword
Power on reset value ???????0HDirect Mapped

Bit(s)	R/W	Name	Function
31:4		UNDEFINED	These bits are undefined.
3:0	R/W	MEMORY PAGE	These bits select what memory page will be accessed. Each memory page is 16 bytes and is addressed from 30H - 3FH.

3.4.CODEC Interface

The CODEC interface register is a 16 bit register that provides access to the CODEC control registers. This register is read only and must be accessed as a word.

CODEC Write RegisterAddress 10H
Addressable as word, longword
Power on reset value ????0000HDirect Mapped

Bit(s)	R/W	Name	Function
31:16		UNDEFINED	These bits are undefined.
15:8	W	ADDRESS	These bits are the address of the CODEC register to be written to.
7:0	W	DATA	These bits are the data value to be written into the CODEC register.

3.5.Serial Interface

There is one 16 bit control register and three 32 bit control/status registers in the serial block. The 16 bit control register can be read or written. The three 32 bit control/status registers can be read or written but only the lower 16 bits can actually be written to. The upper 16 bits of these registers provides the status of the internal sample counter.

Serial Interface Control RegisterAddress 20H
Addressable as byte, word, longword
Power on reset value 00000000HDirect Mapped

Bit(s)	R/W	Name	Function
31:22	R/W	ZERO	These bits always read back as zero. They are not writable.
21:19	R/W	P2_END_INC[2:0]	These bits are the binary offset value that will be added to the sample address counter at the end of the loop. This value is used only if the DAC2 channel is in loop mode it is not used in stop mode. If loop mode is selected this value must be greater than zero otherwise the channel will not function correctly. This minimum value will be one if 8 bit mode is selected and two if 16 bit mode is selected.
18:16	R/W	P2_ST_INC[2:0]	These bits are the binary offset value that will be added to the sample address counter when the channel is started/restarted. This value can be zero and will allow the sample fetch to start on any byte boundary. For 16 bit data this value must be an even number.

15	R/W	R1_LOOP_SEL	This bit selects loop/stop mode for the ADC channel. This bit determines what action the channel will perform when the sample count reaches zero. 0 - Loop mode ; interrupt set (if enabled) but keeps recording 1 - Stop mode ; interrupt set (if enabled) , stops recording
14	R/W	P2_LOOP_SEL	This bit selects loop/stop mode for the DAC2 channel. This bit determines what action the channel will perform when the sample count reaches zero. 0 - Loop mode ; interrupt set (if enabled) but keeps playing 1 - Stop mode ; interrupt set (if enabled) , plays last sample
13	R/W	P1_LOOP_SEL	This bit selects loop/stop mode for the DAC1 channel. This bit determines what action the channel will perform when the sample count reaches zero. 0 - Loop mode ; interrupt set (if enabled) but keeps playing 1 - Stop mode ; interrupt set (if enabled) , plays last sample
12	R/W	P2_PAUSE	This bit selects pause mode for the DAC2 playback channel. When in pause mode the channel will playback the last sample. 0 - Play mode ; normal playback mode or removes channel 1 - Pause mode ; plays last sample continuously on next sample after the pause bit has been set
11	R/W	P1_PAUSE	This bit selects pause mode for the DAC1 playback channel. When in pause mode the channel will playback the last sample. 0 - Play mode ; normal playback mode or removes channel from pause mode on next sample after bit is cl 1 - Pause mode ; plays last sample continuously on next sample after the pause bit has been set
10	R/W	R1_INT_EN	This bit is the interrupt enable bit for the ADC channel. To clear the interrupt this bit must be set to zero and then set to one to enable the next interrupt. 0 - ADC interrupt disabled 1 - ADC interrupt enabled
9	R/W	P2_INTR_EN	This bit is the interrupt enable bit for the DAC2 channel. To clear the interrupt this bit must be set to zero and then set to one to enable the next interrupt. 0 - DAC2 interrupt disabled 1 - DAC2 interrupt enabled
8	R/W	P1_INTR_EN	This bit is the interrupt enable bit for the DAC1 channel. To clear the interrupt this bit must be set to zero and then set to one to enable the next interrupt. 0 - DAC1 interrupt disabled 1 - DAC1 interrupt enabled

7	R/W	P1_SCT_RLD	This bit when set high will force the sample counter for DAC1 to be reloaded with the sample count register value on the next rising edge of the DAC1 left/right clock. This bit can be returned low on the following instruction. It does not have to be held high for more than 1 microsecond. This control bit is rising edge triggered.
6	R/W	P2_DAC_SEN	This bit when set high will enable the DAC2 to continue playback when it is in the stopped condition and the DAC2 channel has been disabled. Without this bit set if the DAC2 channel is disabled it will begin to playback zeros. 0 - DAC2 plays back zeros when disabled 1 - DAC2 plays back last sample when disabled and in stop mode
5:4	R/W	R1_S_EB : R1_S_MB	These two bits select the data format for the ADC channel. For eight bit data modes the msb is always inverted before it is written out to the buffer. For mono modes only the left channel data is recorded. 00 - Eight bit - Mono mode 01 - Eight bit - Stereo mode 10 - Sixteen bit - Mono mode 11 - Sixteen bit - Stereo mode
3:2	R/W	P2_S_EB : P2_S_MB	These two bits select the data format for the DAC2 channel. For eight bit data modes the msb is always inverted after it is read from the buffer. For mono modes the left channel data is duplicated for both the left and right channels. 00 - Eight bit - Mono mode 01 - Eight bit - Stereo mode 10 - Sixteen bit - Mono mode 11 - Sixteen bit - Stereo mode
1:0	R/W	P1_S_EB : P1_S_MB	These two bits select the data format for the DAC1 channel. For eight bit data modes the msb is always inverted after it is read from the buffer. For mono modes the left channel data is duplicated for both the left and right channels. 00 - Eight bit - Mono mode 01 - Eight bit - Stereo mode 10 - Sixteen bit - Mono mode 11 - Sixteen bit - Stereo mode

DAC1 Channel Sample Count RegisterAddress 24H

Addressable as word, longword

Power on reset value 00000000HDirect Mapped

Bit(s)	R/W	Name	Function

31:16	R	CURR_SAMP_CT	These bits are the current value of the internal sample counter for the DAC1 playback channel. The number of samples that have been played is samp_ct - curr_samp_ct.
15:0	R/W	SAMP_CT	These bits are the number of samples minus one that the DAC1 channel will playback.

DAC2 Channel Sample Count RegisterAddress 28H
Addressable as word, longword
Power on reset value 00000000HDirect Mapped

Bit(s)	R/W	Name	Function
31:16	R	CURR_SAMP_CT	These bits are the current value of the internal sample counter for the DAC2 playback channel. The number of samples that have been played is samp_ct - curr_samp_ct.
15:0	R/W	SAMP_CT	These bits are the number of samples minus one that the DAC2 channel will playback.

ADC Channel Sample Count RegisterAddress 2CH
Addressable as word, longword
Power on reset value 00000000HDirect Mapped

Bit(s)	R/W	Name	Function
31:16	R	CURR_SAMP_CT	These bits are the current value of the internal sample counter for the ADC record channel. The number of samples that have been played is samp_ct - curr_samp_ct.
15:0	R/W	SAMP_CT	These bits are the number of samples minus one that the ADC channel will record.

3.6.Host Interface - Memory

The top 64 bytes of memory are actually used as register storage for the CCB block and is also used as the FIFO for the UART block. The CCB registers are located in the lower 32 bytes of this block and require six longwords. These registers control filling the circular buffers for the two playback channels and the record channel. Each channel requires 2 longwords. The UART FIFO is located in the upper 32 bytes of this block and requires all eight longwords but uses only 9 bits of each longword.

DAC1 Frame Register 1Address 30H
Addressable as longword   Memory Page 1100b

Power on reset value ????????HDirect Mapped

Bit(s)	R/W	Name	Function
31:0	R/W	PCI ADDRESS	This longword is the physical PCI address of DAC1 sample buffer in system memory

DAC1 Frame Register 2Address 34H
Addressable as longword Memory Page 1100b
Power on reset value ????????HDirect Mapped

Bit(s)	R/W	Name	Function
31:16	R/W	Current Count	This 16 bit counter indicates the number of longwords that have been transferred.
15:0	R/W	Buffer Size	This 16 bit value indicates the number of longwords in a buffer minus one.

DAC2 Frame Register 1Address 38H
Addressable as longword Memory Page 1100b
Power on reset value ????????HDirect Mapped

Bit(s)	R/W	Name	Function
31:0	R/W	PCI ADDRESS	This longword is the physical PCI address of DAC2 sample buffer in system memory

DAC2 Frame Register 2Address 3CH
Addressable as longword Memory Page 1100b
Power on reset value ????????HDirect Mapped

Bit(s)	R/W	Name	Function
31:16	R/W	Current Count	This 16 bit counter indicates the number of longwords that have been transferred.
15:0	R/W	Buffer Size	This 16 bit value indicates the number of longwords in a buffer minus one.

ADC Frame Register 1Address 30H
Addressable as longword Memory Page 1101b
Power on reset value ????????HDirect Mapped

Bit(s)	R/W	Name	Function

31:0	R/W	PCI ADDRESS	This longword is the physical PCI address of ADC sample buffer in system memory

ADC Frame Register 2Address 34H
Addressable as longword Memory Page 1101b
Power on reset value ????????HDirect Mapped

Bit(s)	R/W	Name	Function
31:16	R/W	Current Count	This 16 bit counter indicates the number of longwords that have been transferred.
15:0	R/W	Buffer Size	This 16 bit value indicates the number of longwords in a buffer minus one.

UART FIFO Register Address 30, 34, 38, 3CH
Addressable as longword Memory Pages 1110, 1111b
Power on reset value ????????HDirect Mapped

Bit(s)	R/W	Name	Function
31:9	R/W	OPEN	These bits are not used.
8	R/W	BYTE VALID	This bit indicates whether the UART byte contains valid data. 0 - UART byte not valid 1 - UART byte valid
7:0	R/W	UART BYTE	This byte is a byte the has been received by the UART block through the MIDI interface.

POWER MANAGEMENT

All power management of the system is under software control. The CODEC and AudioPCI™ can be powered down separately. Neither chip loses register information when powered down.

The AudioPCI™ can be power managed by shutting down various sub-systems. We can power down the following blocks: Joystick, UART, CODEC Interface, Serial Interface. The AudioPCI™ Clock generator, CCB, IRQ and PCI Interface remain in a powered up condition.

During operation, the CODEC has typical power dissipation of 315mW and AudioPCI™ is 100mW. In power down, the CODEC is 100mW, and AudioPCI™ is 15mW.

3.7.CODEC Power Management

The CODEC is powered down by setting bit 1 (of control bits 7 - 0) in control register 16 (hex) to a zero. The CODEC control registers are written through the CODEC Interface block at address 10 (hex). For details refer to the AKM4531 CODEC specification and also the CODEC Interface section (7.4) of this specification.

3.8.AudioPCI™ Power Management

As mentioned above, the Joystick, UART, CODEC Interface and Serial Interface blocks of the AudioPCI™ chip can be individually powered down. The AudioPCI™ Clock generator, CCB, IRQ and PCI Interface remain in a powered up condition. AudioPCI™ is powered down by setting bits 6 - 1 (of control bits 31 - 0) to zero. The AudioPCI™ control register is located in the IRQ and Chip Select Block at address 00 (hex). For details refer to the IRQ and Chip Select Block section (7.1) of this specification. Note that the Serial Interface actually has three separate enable bits, one for each of the playback channels and one for the record channel.

4.PCI BUS Description and Signals

AudioPCI™ is designed to adhere to the PCI Local Bus Specification Revision 2.1, as such it complies with all requirements for bus master capability. It is a 32 bit device and does not currently support the optional 64 bit bus modes. Of the optional pins described in the PCI specification, AudioPCI™ only uses Interrupts. Although the Sample buffer space is referred to as cache, it is not the system memory cache described in the PCI specification. This cache is a local sound memory cache and is not part of the directly accessible system memory. **Note:** The „#“ symbol indicates a low active signal.

4.1.Parity

AudioPCI™ implements the PAR signal. This signal is an even parity check described in the PCI specification. AudioPCI™ will generate PAR whenever it drives AD[31:0]. Although AudioPCI™ will generate PAR , it will not generate the Bus Error condition signals PERR# and SERR# due to parity errors. This exception is allowed in the PCI Specification section 3.8.2.

4.2.LOCK#

AudioPCI™ does not support PCI bus lock functions.

4.3.Bus Speed

Since AudioPCI™ uses a high speed intermediate buffer to transfer data to and from the PCI bus, it runs at the standard 33MHz. Rate. However, it is believed that the memory speed on the PCI bus may limit the transaction rate by inserting one wait state. All latency calculations are based on this assumption.

5.PIN DESCRIPTION

5.1.PCI Interface

The PCI Interface follows the information presented on the PCI Local Bus Specification Revision 2.1. For a more complete description of each of the PCI signal please refer to the PCI specification.

CLK Clock: A 33MHz input signal from the PCI bus. This is the master timing control for all PCI transfers.

RST# Reset: The device will essentially be in sleep mode after reset.

AD[31:0]The Address/Data multiplexed signals of the PCI Bus.

C/BE#[3:0]Bus Command and Byte Enables. Define the type of transfer that will take place.

FRAME#Cycle Frame. Driven by the current bus master, this signal indicates the beginning of a transfer. When FRAME# is deasserted, the transaction is in the final phase.

IRDY#Initiator Ready. This signal indicates that the initiating agent (the bus master) is able to accept the data phase of the transaction. Normally used to create wait states by the master.

TRDY#Target Ready. Driven by the target (the selected device), this signal indicates that the target is ready for the data transaction. Generally used to generate wait states by the target.

STOP#Stop indicates the current target is requesting the master to stop the current transaction.

SERR#System Error.

PARThe Parity signal is even parity. The number of „1"s on AD[31:0],C/BE[3:0] and Par equal an even number.

IDSELInitialization Device Select. This signal is used as a chip select during configuration read and write transactions

DEVSEL#Device Select. This signal, when actively driven, indicates that the driving device has decoded its address as the target of the current transaction.

REQ#Request indicates to the arbiter that AudioPCI™ desires use of the bus.

GNT#Grant. This signal indicates that control of the PCI Bus has been granted and AudioPCI™ is now the bus master.

INTA#AudioPCI™ supplies interrupt support for all possible interrupt configurations. This is done so that the greatest possible flexibility can be achieved during the configuration process.

5.2.CODEC Interface

CDATACODEC Serial Control Data

CCLKCODEC Serial Control Clock

CCS#CODEC Serial Control Chip Select

CBUSYCODEC Serial Control Busy

CSDOData from CODEC A/D Converter

CMCLK1Master Clock for D/A #1
CLRCLK1Left/Right Clock for D/A #1
CBCLK1Bit Clock for D/A #1
CSERDIN1Data to D/A #1
CLRCLK2Left/Right Clock for D/A #2 and A/D
CBCLK2Bit Clock for D/A #2 and A/D
CSERDIN2Data to D/A #2

5.3.Miscellaneous

JOY[7:0]Joystick and Button inputs
MIDI_OUTSerial RS232 output for MIDI compatible communications
MIDI_INSerial RS232 input for MIDI compatible communications
XTALIN/OCrystal input and output
XIRQ/XCTL1External IRQ output for platform NMI routing , or a general purpose output
MUTEExternal output bit that controls muting the audio outputs
MPEG_LRCLKExternal source (MPEG) I2S left/right clock input
MPEG_BCLKExternal source (MPEG) I2S bit clock input
MPEG_DATAExternal Source (MPEG) I2S serial data input

5.4.Power Supplies

VDDDigital Supply Voltage
VSSDigital Ground pins

6.PINOUT.

7.

TIMING.

AudioPCI™ is being designed to conform to the PCI Local Bus Specification Revision 2.1. Since AudioPCI™ has a high speed intermediate 8 LWORD RAM buffer, the design target is to have no wait states on the data transfers. This level of performance is currently being evaluated. The fab being used is supplying this PCI prototype cell, already in silicon for evaluation. Ensoniq will make the determination on the final timing after the evaluation has been completed.

For detailed information on the PCI timing for AudioPCI™ please refer to section 3.3 Bus Transactions in the PCI Specification.

The timing information for the signals from the AudioPCI™ to the CODEC can be found in the AKM 4531 Specification.

8.DC Characteristics

The DC characteristics for AudioPCI™ conform to the DC specification for the PCI bus. This data will be added to the next specification revision..

9.Mechanical Information

APPENDIX

9.1.Bus Latency

Since each audio channel has a 64 byte buffer, the Latency requirement for the PCI bus can be calculated as follows:

For 8 bit audio: 32 Samples (one half buffer) @ 44.1 kHz. = 725msec.
For 16 bit audio:16 Samples @ 44.1 kHz. = 363 msec.

Therefore, once a Bus Request is made, AudioPCI™ needs to have the PCI bus grant in 363 msec. for 16 bit samples. In most game environments the sound effects are 8 bit and the high latency figure is acceptable. If more than one channel needs servicing, this does not impact the latency calculation because once the PCI Bus is granted it can be held until all channels are serviced. Since AudioPCI™ uses 8 Long Word burst transfers, each channel is filled with one burst transfer and AudioPCI™ can service all three with just 24 transfers.

9.2.Bus Bandwidth

The Bus bandwidth required by AudioPCI™ is very low. If all three channels are running at 44.1 kHz the total bandwidth is:

44.1 kHz ´ 2 (stereo) ´ 3 (channels) ´ 2 (bytes) = 529 KBytes/sec.

This represents less than 0.5% of the available PCI Bus bandwidth.